OV2640 Camera Module

Hardware Application Notes

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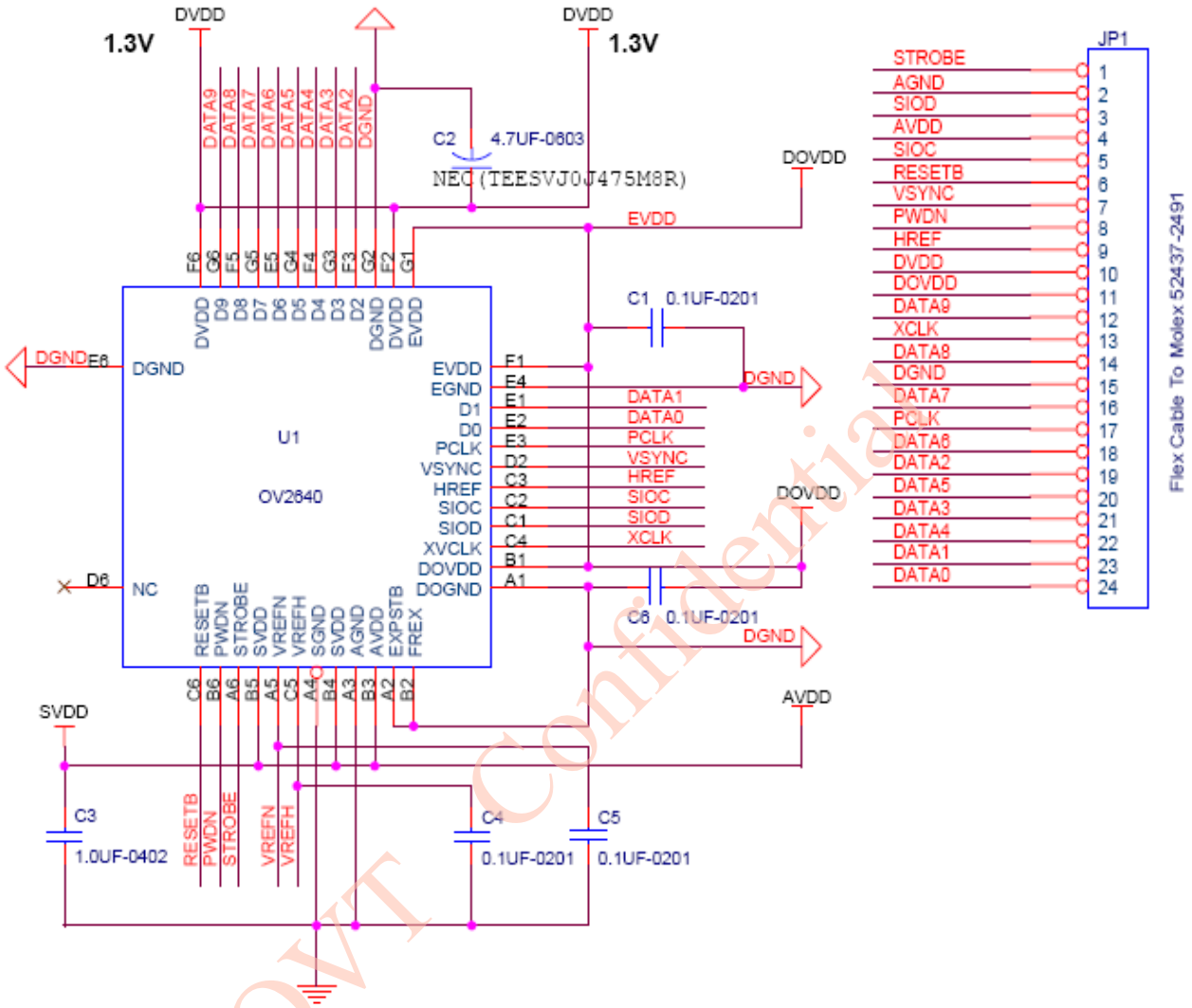
1. OV2640 Camera Module Reference Design



NOTE:
Connector PWDN should be connected to ground if unused.
Sensor reset pin RESETB is active low.
AVDD is 2.8V sensor analog power.
DVDD is 1.3V sensor digital power.
DOVDD is 1.8V to 3.0V sensor digital IO power.
Sensor AGND and DGND should be separated and connect to a single point at outside PCB (Don't connect inside module).
C2 should close to sensor DVDD and DGND.
C3 should close to sensor SVDD, AVDD and AGND.
C4 should close to sensor VHRFH and AGND.
C5 should close to sensor VREFN and AGND.
C6 should close to sensor DOVDD and DGND.
C1 should close to sensor EVDD and DGND.
D9:D2 is module YUV and RGB 8bits output (D9:MSB, D2:LSB).
D9:D0 is module raw RGB 10 bits output (D9:MSB, D0:LSB

2. OV2640 Camera Interface Reference for Camera Phone

2.1 Pin Definition

OV2640 has 10-bit video port, D[9:0]. For 10-bit RGB raw output, D[9:0] are used. **For 8-bit YCbCr, 8-bit RGB raw or 8-bit RGB 565 output, only D[9:2] are used.**

The Href and Hsync signal is on the same pin – Href pin. The function of this pin could be selected as either Href function or Hsync function by SCCB setting.

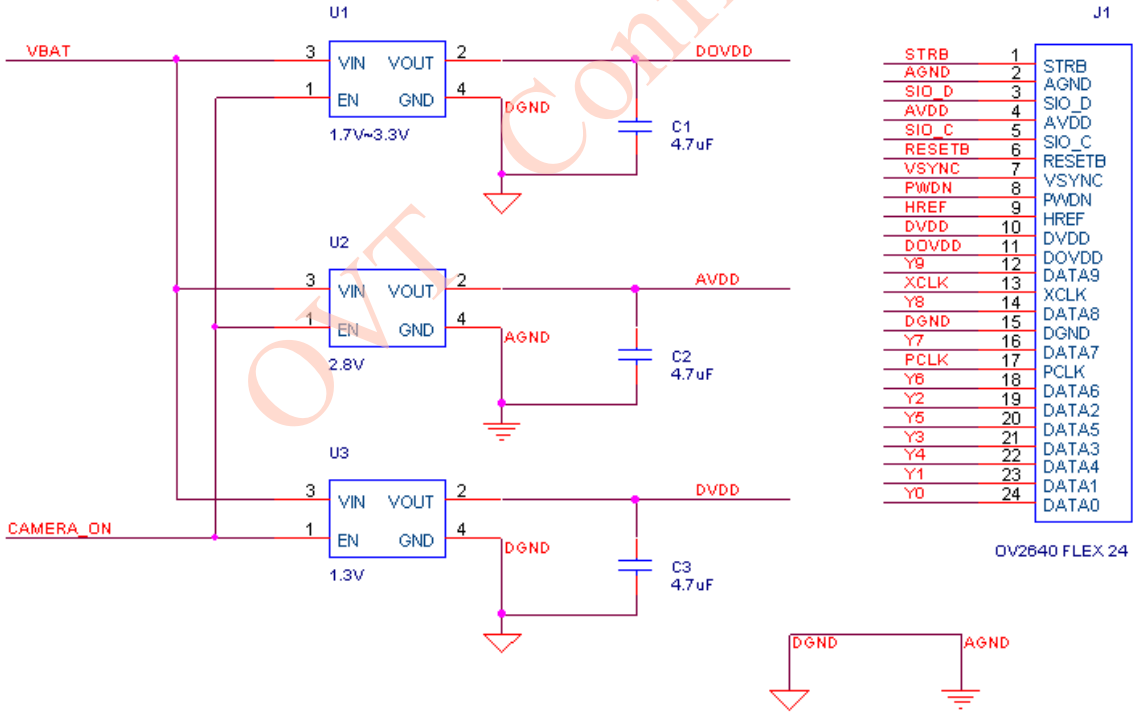
The SIO_C and SIO_D bus should have external pull up resistors, the typical value of the pull up resistors is about 4.7K.

Resetb is active low. There is no internal pull-down/pull-up resistor. It can be controlled by a GPIO, or connected to DOVDD using an external pull-up resistor if not used. If Resetb is connected to DOVDD, the OV2640 camera module could be reset by SCCB setting.

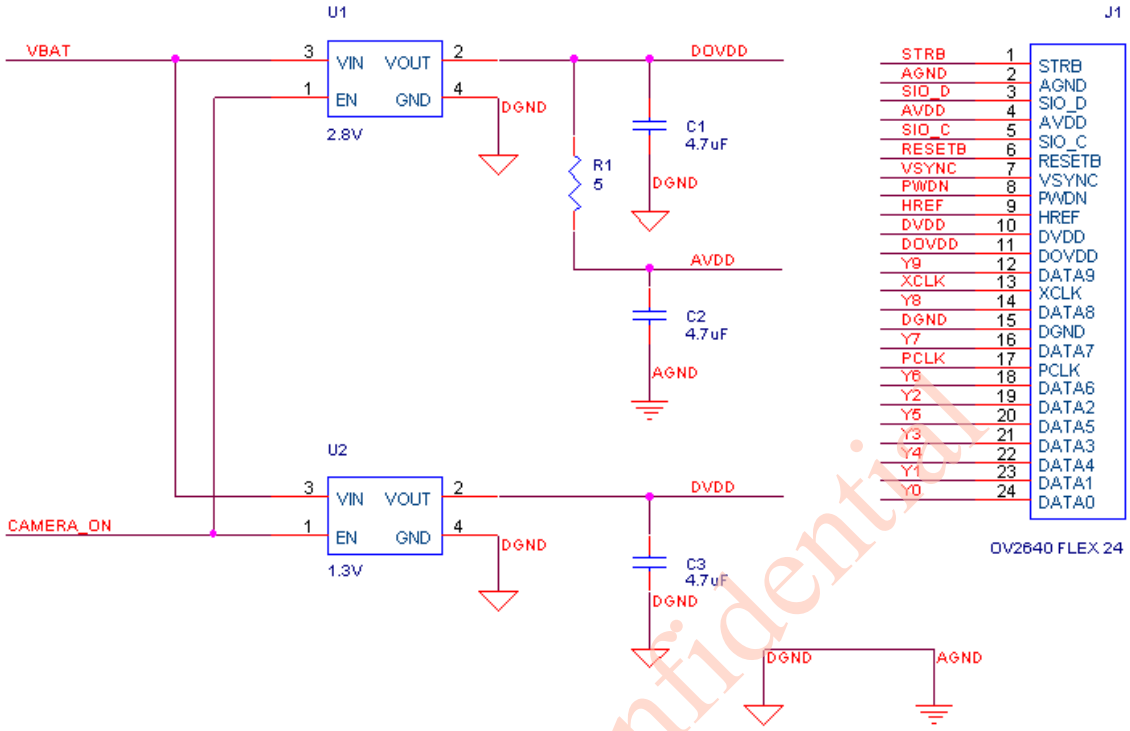
PWDN is active high. There is no internal pull-down/pull-up resistor. It can be controlled by a GPIO, or connected to DGND using an external pull-down resistor if not used.

2.2 Power Supply

If DOVDD uses different power supply than AVDD, then 3 regulators should be used.



If DOVDD uses the same voltage as AVDD, then only 2 regulators are required. R/C filter is used to separate AVDD from DOVDD.



Please note that:
a. The AGND and DGND should be separate inside module and connected together on phone PCB very close to camera module connector.

3. OV2640 Camera Operation

3.1 Power Saving Modes

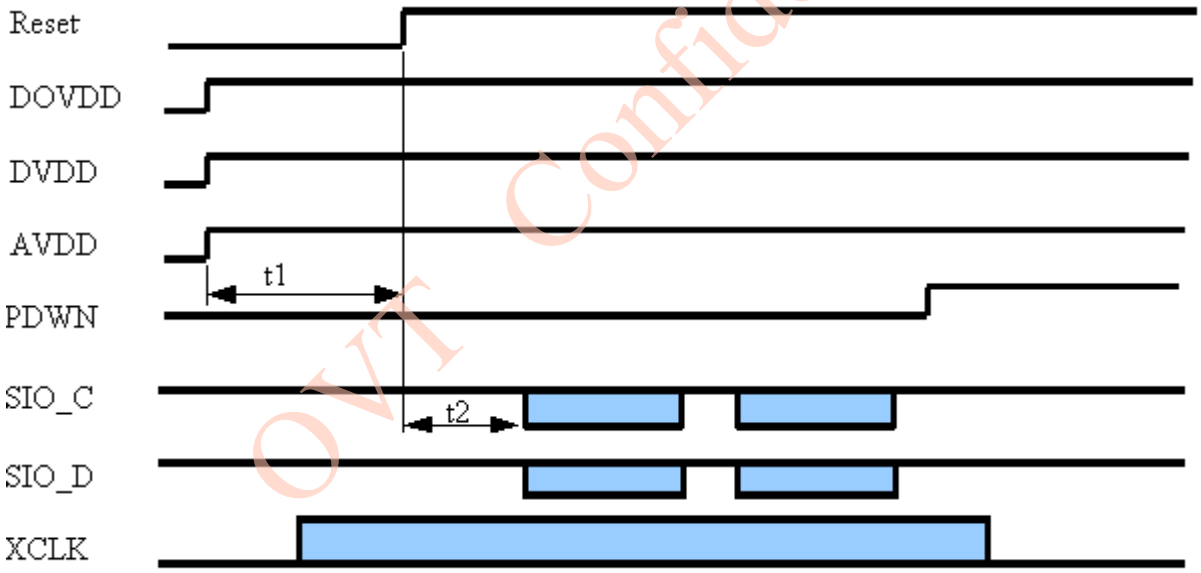
There are 2 kind of power saving modes: power down mode and power off mode.

Power down mode means that in power saving mode, all the power supplies to the camera module are kept. The camera is set into power down mode by pull high PWDN. **For OV2640, there have big power down current, so power down mode is not supported by OV2640 for power saving.** But power down mode is still useful if OV2640 shares SCCB bus with other devices or OV2640 shares video bus with another camera for camera applications. So OV2640 power operation in power down mode is still introduced here.

Power off mode means that in power saving mode, all the power supplies to the camera module are cut.

3.2 Camera Operation in Power Down Mode

3.2.1 Battery On, Hardware Reset



t1: from powers on to Reset pull high, >= 3ms
t2: from Reset pull high to SCCB initialization, >= 3ms

Step 1:

Reset is applied to OV2640 camera module.

Step 2:

DOVDD, DVDD and AVDD powers are applied. The 3 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, DVDD second and AVDD

last.

Step 3:
after 3ms of last power applied, pull high Reset.

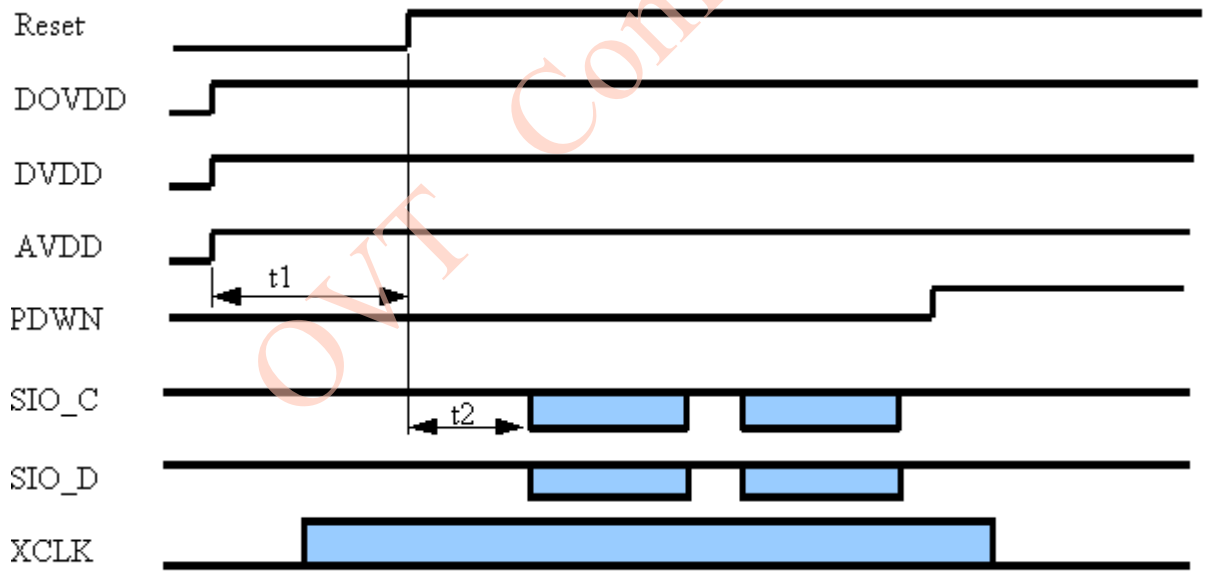
Step 4:
After 3ms, initialize OV2640 by SCCB initialization. Please find initialization setting from "OV2640 Camera Module Software Application Notes" or contact OmniVision local FAE.

Step 5:
Pull high PWDN. Set OV2640 to power down mode.

Step 6:
Pull XCLK low.

After battery on, OV2640 cameras should be set to power down mode to minimize power consumption. The cameras should be initialized first, then set to power down mode.

3.2.2 Battery On, Software Reset



t1: from powers on to SCCB software reset, >= 3ms
t2: from software reset to SCCB initialization, >= 2ms

Step 1:
DOVDD, DVDD and AVDD powers are applied. The 3 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, DVDD second and AVDD last.

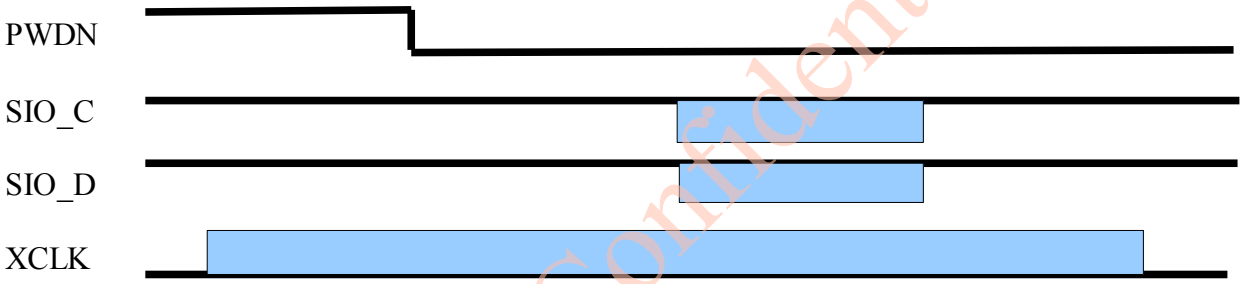
Step 2:
after 3ms of last power applied, reset OV2640 camera module by SCCB write.

Step 3:
After 2ms, initialize OV2640 by SCCB initialization. Please find the initialization setting from "OV2640 Camera Module Software Application Notes" or contact OmniVision local FAE.

Step 4:
Pull high PWDN. Set OV2640 to power down mode.

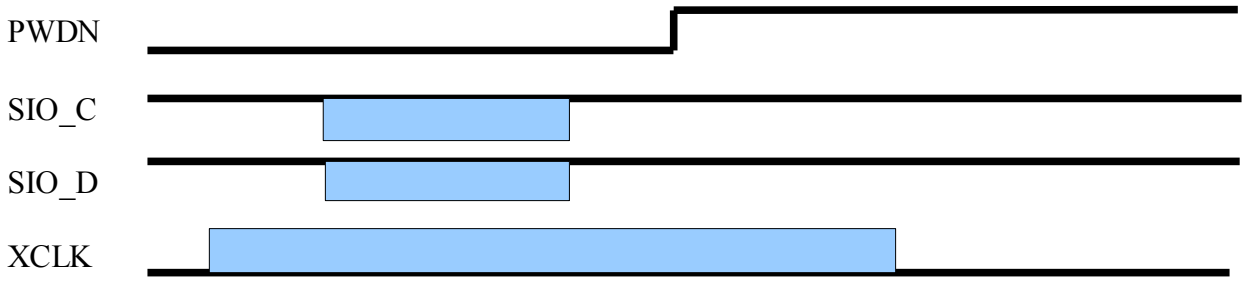
Step 6:
Pull low XCLK.

3.2.3 Wake up From Power Down



Step 1:
Apply XCLK
Step 2:
after 10ms, Pull Low PWDN
Step 3:
Optional Step 4:
Initialization.

3.2.4 Power Down



Step 1:
Pull PWDN pin high.

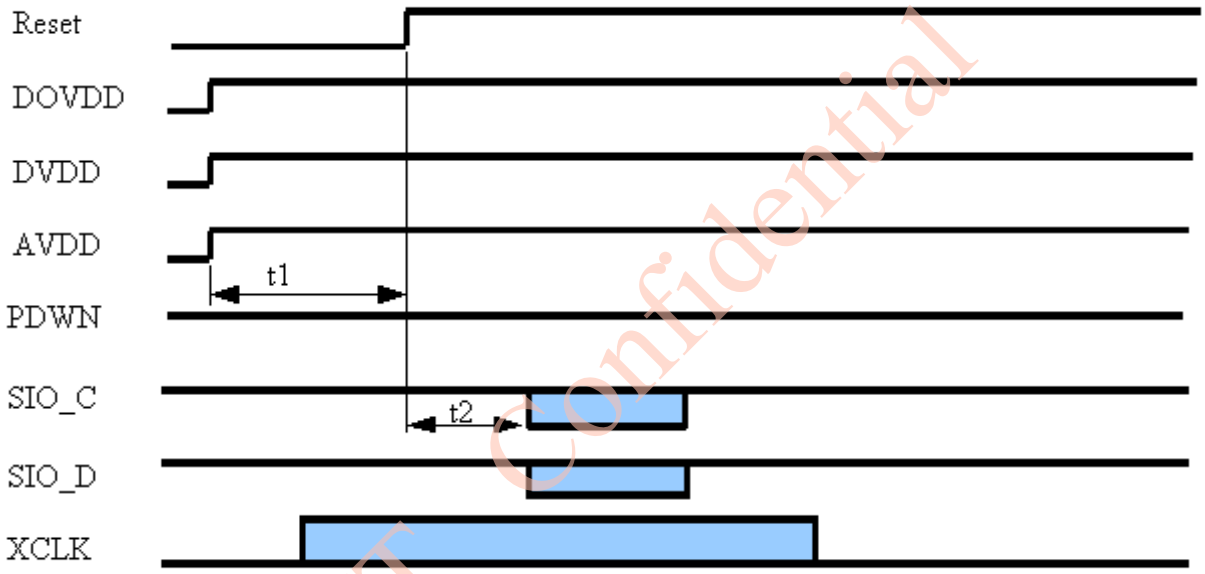
Step 2:
Pull XCLK low

3.3 Camera Operation in Power Off Mode

3.3.1 Battery On

No operation. Camera module is power off.

3.3.2 Camera On, Hardware Reset



t1: from powers on to SCCB software reset, >= 3ms
t2: from software reset to SCCB initialization, >= 2ms

Step 1:
Reset is applied to OV2640 Camera Module.

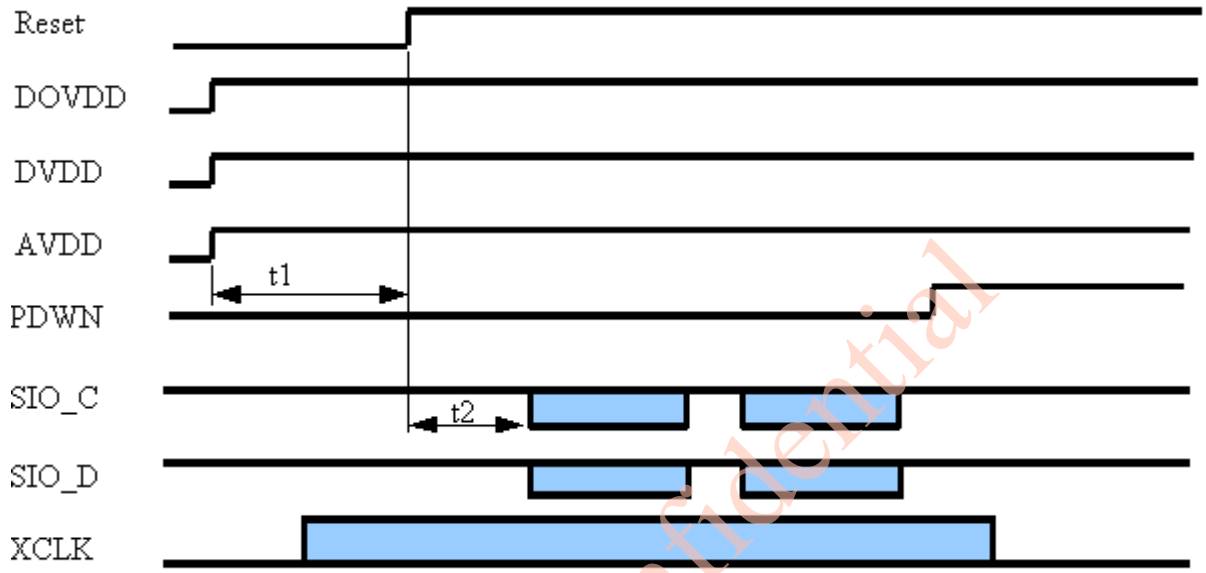
Step 2:
DOVDD, DVDD and AVDD powers are applied. The 3 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, DVDD second and AVDD last.

Step 3:
after 3ms of last power applied, pull high Reset.

Step 5:

After 3ms, initialize OV2640 by SCCB initialization. Please find initialization setting from "OV2640 Camera Module Software Application Notes"or contact OmniVision local FAE.

3.3.3 Camera On, Software Reset



t1: from powers on to SCCB software reset, >= 3ms
t2: from software reset to SCCB initialization, >= 2ms

Step 1:

DOVDD, DVDD and AVDD powers are applied. The 3 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, DVDD second and AVDD last.

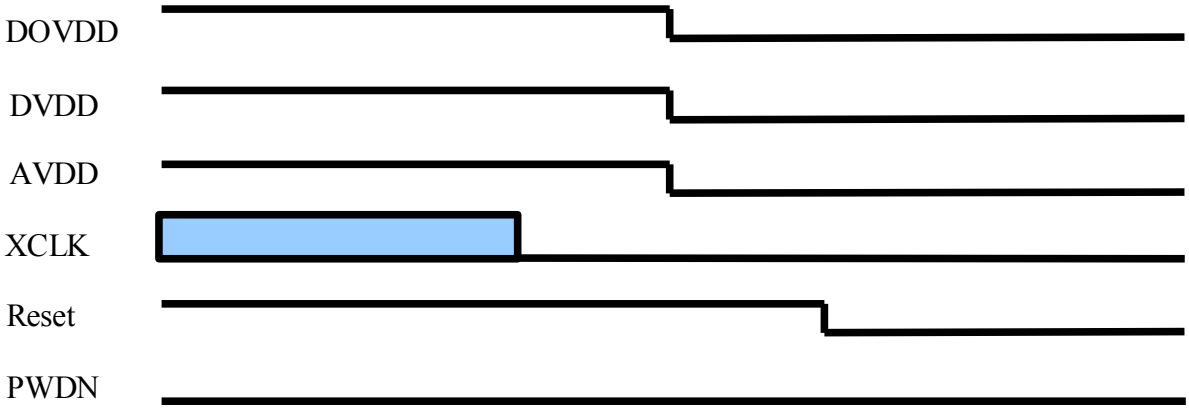
Step 2:

after 3ms of last power applied, reset OV2640 camera module by SCCB write.

Step 3:

After 2ms, initialize OV2640 by SCCB initialization. Please find initialization setting from "OV2640 Camera Module Software Application Notes" or contact with OmniVision local FAE.

3.3.4 Camera Off



Step 1.

Pull low XCLK,

Step 2.

Turn off AVDD, DVDD and DOVDD. The 3 powers could be turned off simultaneously. If turned off separately, AVDD should be turned off first, DVDD second and DOVDD third.

Step 3.

Pull Low PWDN and RESET

4. SCCB Bus sharing

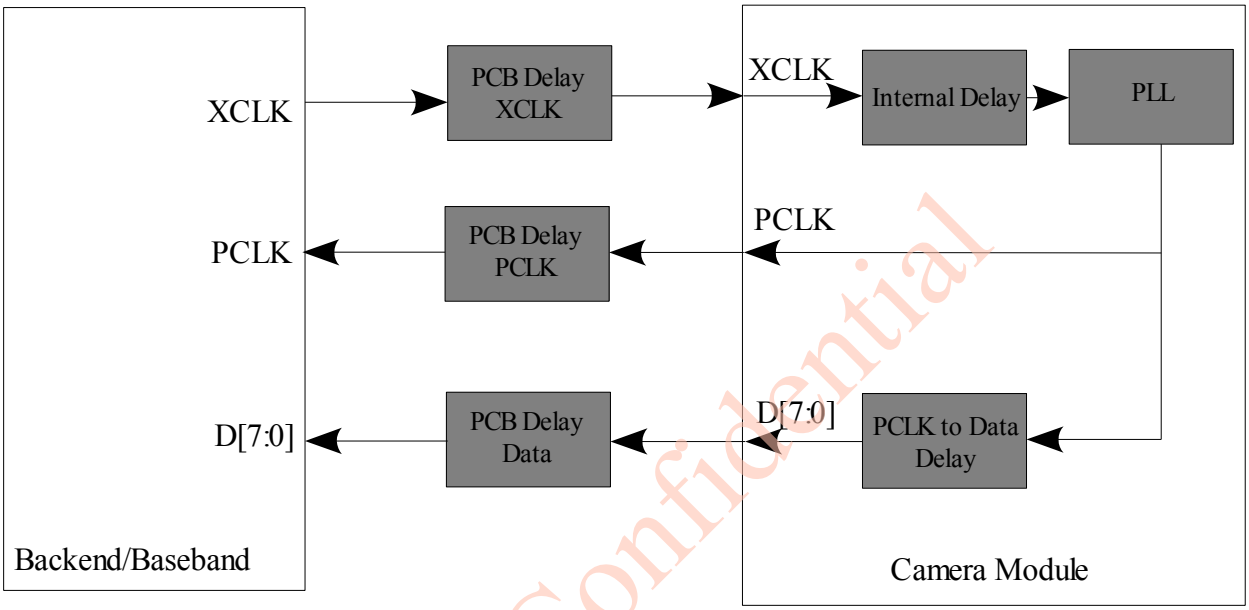
The SCCB bus of OV2640 camera module could share with other SCCB device. When OV2640 is working, the read/write operation is separated by device address. The device address of OV2640 is 0x60. SCCB read/write to address other than the 2 address above will not affect SCCB registers of OV2640.

The SCCB bus of OV2640 could be shared with other devices in both power down mode and power off mode. When OV2640 camera module is power down or power off, the SCCB Bus is leave free. The SCCB of OV2640 doesn't affect the read/write of other SCCB device.

5. Timing Considerations for Phone PCB Design

There are 2 clock signal for OV2640 camera module. One is the main clock (input clock) XCLK, the other is the pixel clock (output clock) PCLK. Some backend/baseband chips may use XCLK as pixel sample clock, some backend/baseband chips may use PCLK as pixel sample clock. **It is recommended to use PCLK as pixel sample clock.**

Let's look at the clock distribution first.



So the delay of video data to clock at backend/baseband side is very critical for timing design. If the delay is over the spec. of backend/baseband chip, the backend/baseband chip can not get video data correctly. The incorrect video data may have wrong color, fixed or moving horizontal lines.

From the clock distribution diagram above, the delays are:

Delay_XCLK = 0

Delay_PCLK = PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCB_Delay_PCLK

Delay_Data = PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCLK_to_Data_Delay + PCB_Delay_Data

5.1 Sample with PCLK

If Backend/baseband sample video data with PCLK, the clock data delay is

clock_data_delay = Delay_Data – Delay_PCLK

= PCLK_to_Data_Delay + PCB_Delay_Data – PCB_Delay_PCLK

The clock data delay is not related with PCB delay of XCLK.

If PCB is carefully designed so that the wire length of PCLK and Data are same, then PCB_Delay_Data = PCB_Delay_PCLK, the clock data delay is

clock_data_delay = PCLK_to_Data_Delay, not related to PCB layout

5.2 Sample with XCLK

If Backend/baseband sample video data with PCLK, the clock data delay is

clock_data_delay = Delay_Data – Delay_XCLK

= PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCLK_to_Data_Delay + PCB_Delay_Data

The data to clock delay at Baseband/Backend chip are much bigger than sampled with PCLK. And the delay is highly depend on PCB layout. So if XCLK is used to sample video data, it is very likely to have timing issue which would cause incorrect video data.

5.3 Using EMI/ESD Device

If EMI/ESD device are used in phone design, the PCB delay increase very much. It should be very careful to manipulate the delays to meet timing spec. of backend/baseband chips.

1. Try to use PCLK as sample clock of video data.
2. XCLK and PCLK should not share ESD/EMI device with other signals. Use dedicate ESD/EMI device or R/C filters for XCLK and PCLK. So that the delay on XCLK and PCLK could be adjusted later.
3. For camera module, use single ESD/EMI device or single R/C filter for XCLK and PCLK to minimize clock delay.
4. Carefully layout PCB to keep XCLK wire as short as possible, PCLK wire the same length as data lines.
5. Minimize the length of FPC of camera module.

6. Hardware Check List

6.1 Check Hardware Design

6.1.1 Module Function

Check camera module function with USB 2.0 test board (Module interface board may be needed, please contact with module maker). The module should display image correctly on PC.

Check module schematic design, pin definition match with camera interface of phone. Analog ground and digital ground are separated inside camera module.

6.1.2 Check Camera Interface of Phone

Pin definition matches with camera module design.

AVDD is supplied by separate regulator. DVDD and DOVDD could be supplied by separate regulator or shared regulator with other circuits. The voltage of each power supplied are within sensor specification.

If there is a long flex cable to connect camera module to main board of phone, please make sure the ground of camera module is not shared with other circuits. For flip type phone, share camera ground with LCD module would cause very strong power/ground noise.

6.2 Check if Camera Module is Working

Evidence of camera module working

PCLK output

HREF, VSYNC outputs

D[9:0] output

Check procedures

a. Voltages of power supplies are within sensor specification

b. input clock is correct

c. all input signals are in correct state

PWDN = in active, Reset = in active, SIO_D = H, SIO_C = H

d. for OV2640 and later, please check SCCB initialization waveform to make sure SCCB initialization is completed.

If all the check are passed, the camera module still can not work, please check if the camera module is damaged or contact OmniVision local FAE.

6.3 Check SCCB

a. Check SCCB connection: Pull up resistors exist. Recommended value is around 4.7K.

b. SCCB write speed should not be too fast for first debug. Recommended not over 100K. The write speed could be increased up to 400K later on.

c. Simple ways to check SCCB

SCCB read could be verified by read register 0x0a, 0x0b (version).

SCCB write could be verified by write register 0x11 and check PCLK frequency.

d. To make sure SCCB read/write are correct, please use oscilloscope to capture whole waveforms of SCCB initialization.

e. Make sure the SCCB device ID is correct for read/write operation.

SCCB address is 0x60/0x61 for 1.3M and above sensors

f. If SCCB soft reset is used, please wait at least 2~5ms after SCCB soft rest.

6.4 Check Camera Interface

a. Check polarity of HREF(HSYCN), VSYNC, PCLK, make sure the polarity of camera module matches with backend or baseband side.

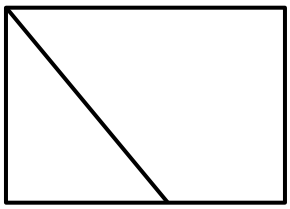
b. Check sample clock. Please pay attention to baseband/backend sample with MCLK. In this case, the clock divider inside sensor could not be turned on. Please also pay attention to possible timing issues listed in section 5.

c. check window position.

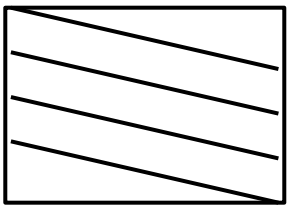
If camera interface uses HREF, then the window position is defined by sensor.

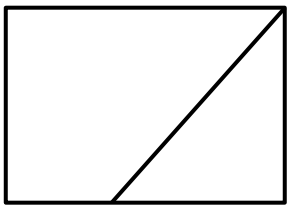
If camera interface uses HSYNC, then the window position is defined by backend / baseband.

6.5 Some Typical Issues

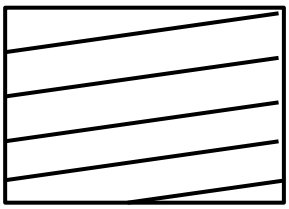


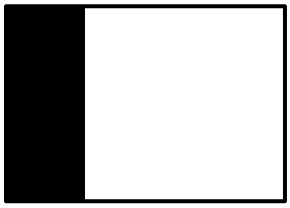
Line width too big





Line width too small

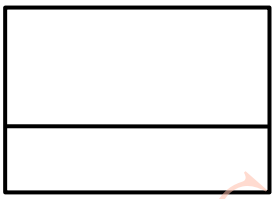




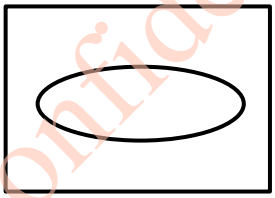
Wrong Window Position

In sufficient output lines

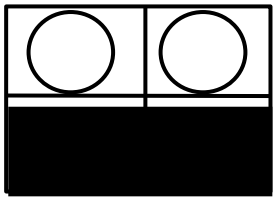
Horizontal Sync Issue



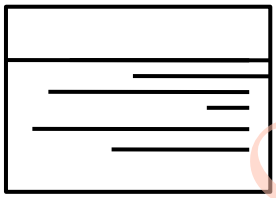
Vertical Sync Issue



Sample Rate too High



Sample rate too low



Timing Issue

6.6 Image Direction

6.6.1 Sensor 4:3, LCD 3:4

Full screen display is not full view angle

Full view angle display is not full screen

Full view angle

Full Screen

Camera module

6.6.2 Sensor 3:4, LCD 3:4

Sensor rotate 90 degree in camera module

Picture scan line direction should be changed by phone

Full Screen and Full view angle on LCD

Full view angle & Full Screen

Change scan line direction of camera

6.7 Check Color/Brightness

a. There are only red/green color in picture

Y and U/V exchanged.

b. R/B exchange

U/V exchange

c. color/brightness not continuous

check connection of d[9:0]

6.8 Check Image Center

Place an object in front of camera module, check if the picture is on center of LCD. If not, the output window of camera is not correct.